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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/955,704	09/19/2001	Gregory E. Ehmann	VLSI.323PA	9776

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EXAMINER	
WILSON, YOLANDA L	

ART UNIT	PAPER NUMBER
2113	

DATE MAILED: 07/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/955,704	EHMANN ET AL.	
	Examiner	Art Unit	
	Yolanda Wilson	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 September 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 January 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to because Figure 2 was not sent in the January 24, 2002 communication of Formal drawings to be entered. Only Figure 1 was received. Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

2. Claim 27 is objected to because of the following informalities: Claim 27 is objected to because it depends upon claim 26, which does not include the subject matter 'test-traffic type'. Examiner believes that claim 26 is supposed to

be dependent upon claim 22 and will reject this claim as being dependent upon claim 22. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-17,19-25,27,28 are rejected under 35 U.S.C. 102(e) as being anticipated by Fruehling et al. (USPN 6625688B1). As appears in claim 1, Fruehling et al. discloses a data-generation circuit adapted to provide a first data stream; a memory arrangement adapted to buffer a plurality of programmable commands, the programmable commands indicative of at least one of test-traffic type, pattern and behavior-in-time; state machine circuitry coupled between the memory arrangement, the data-generation circuit and the digital data path, the state machine circuitry adapted to assemble portions of the first data stream into test-traffic wherein at least one of type, pattern and behavior-in-time is selected responsive to the programmable commands, and further adapted to generate test-traffic on the digital data path; and a status and feedback circuit adapted to monitor the digital data path for test-traffic and generate a feedback signal indicative of at least one of test-traffic throughput and test-traffic quality in column

9, line 26 – column 10, line 4. The data generation circuit is the LFSR. The state machine circuitry is the bus control logic. The status and feedback circuit is the parallel signature analyzer.

5. As per claim 2, Fruehling et al. discloses wherein the state machine circuitry includes a command state machine and a bus master state machine, the command state machine being coupled to the memory arrangement and data-generation circuit, and adapted to direct the bus master state machine to assemble portions of the first data stream into test-traffic having pre-defined type, pattern and behavior-in-time responsive to the programmable commands, and the bus master state machine is coupled to the digital data path and adapted to communicate the test-traffic onto the digital data path responsive to the command state machine in Figure 2 and column 9, lines 26-34. The bus control logic includes the bus master state machine and the command state machine.

6. As per claim 3, Fruehling et al. discloses wherein the state machine circuitry is adapted to assemble portions of the first data stream into a test-traffic type selected from a group consisting of 1, 2, 4, 8, 16, 32, and 64 words per burst in column 9, lines 26-34 and column 13, lines 13-28.

7. As per claim 4, Fruehling et al. discloses wherein the state machine circuitry is adapted to assemble portions of the first data stream into a test-traffic type selected from a group consisting of other than 1, 2, 4, 8, 16, 32, and 64 transfers per burst in column 9, lines 26-34 and column 14, lines 40-47.

8. As per claim 5, Fruehling et al. discloses wherein the state machine circuitry is further adapted to receive the first data stream from the data-

generation circuit without generating test-traffic on the digital data path in column 9, lines 26-34 and column 13, lines 13-28.

9. As per claim 6, Fruehling et al. discloses wherein the state machine circuitry is adapted to pause in response to programmable commands in column 10, lines 58-60. The bus control logic would be paused if a fault occurred.

10. As per claim 7, Fruehling et al. discloses a bus interface circuit coupled between the memory arrangement and the digital data path, the bus interface circuit adapted to pass programmable commands received via the digital data path to the memory arrangement in column 9, lines 26-34.

11. As per claim 8, Fruehling et al. discloses wherein the first data stream is a repeatable sequence of binary data in column 10, lines 19-33.

12. As per claim 9, Fruehling et al. discloses the data-generation circuit is a second memory arrangement, the first data stream being stored in the second memory arrangement in column 9, line 47 – column 10, line 4.

13. As per claim 10, Fruehling et al. discloses wherein the first data stream comprises a sequence of pseudo-random numbers in column 10, lines 19-33.

14. As per claim 11, Fruehling et al. discloses wherein the data-generation circuit is a second memory arrangement, the first data stream being stored in the second memory arrangement in column 9, line 47 – column 10, line 4.

15. As per claim 12, Fruehling et al. discloses wherein the data-generation circuit is a linear feedback shift register (LFSR) circuit, the first data stream comprising a sequence of LFSR values in column 9, line 47 – column 10, line 4.

16. As per claim 13, Fruehling et al. discloses wherein the state machine circuitry is configured and arranged to seed the LFSR and control content of the first data stream in column 9, lines 26-34.

17. As per claim 14, Fruehling et al. discloses wherein the status and feedback circuit is further adapted to verify monitored test-traffic against corresponding LFSR values, and the feedback signal being an interrupt generated indicative of the test-traffic verification in column 9, line 47 – column 10, line 4.

18. As per claim 15, Fruehling et al. discloses wherein the status and feedback circuit is further adapted to verify monitored test-traffic against a corresponding first data stream, and the feedback signal being an interrupt generated indicative of the test-traffic verification in column 9, line 47 – column 10, line 4.

19. As per claim 16, Fruehling et al. discloses wherein the memory arrangement includes command registers adapted to store programmable commands, configuration registers adapted to store traffic generation process control information and status registers adapted to store test-traffic verification information in column 9, line 26 – column 10, line 4.

20. As per claim 17, Fruehling et al. discloses wherein the status and feedback circuit includes a counter adapted to specify a number of command repetitions, and a loop timer adapted to specify a period within which a set of programmable commands must execute in column 12, lines 15-60.

21. As per claim 19, Fruehling et al. discloses a digital data path; a plurality of traffic sources, each traffic source coupled to the digital data path and adapted to communicate non-test-traffic onto the digital data path; and a circuit arrangement for generating test-traffic coupled to the digital data path, the circuit arrangement including, a data-generation circuit adapted to provide a first data stream, a memory arrangement adapted to buffer a plurality of programmable commands, the programmable commands indicative of at least one of test-traffic type, pattern and behavior; state machine circuitry coupled between the memory arrangement, the data-generation circuit and the digital data path, the state machine circuitry adapted to assemble portions of the first data stream into test-traffic wherein at least one of type, pattern and behavior-in-time is selected responsive to the programmable commands, and further adapted to generate test-traffic on the digital data path; and a status and feedback circuit adapted to monitor the digital data path for test-traffic and generate a feedback signal indicative of at least one of test-traffic throughput and test-traffic quality, wherein at least one of the plurality of traffic sources is a processor circuit in Figure 2 and in column 9, line 16 – column 10, line 4. The traffic sources are the cpu's. The data generation circuit is the LFSR. The state machine circuitry is the bus control logic. The status and feedback circuit is the parallel signature analyzer.

22. As per claim 20, Fruehling et al. discloses wherein the data-generation circuit is a linear feedback shift register (LFSR) circuit, the first data stream consists of a sequence of pseudo-randomly generated binary numbers representing LFSR values in column 10, lines 19-33.

23. As per claim 21, Fruehling et al. discloses wherein the status and feedback circuit is further adapted to verify monitored test-traffic against a corresponding first data stream, and the feedback signal is an interrupt generated indicative of the test-traffic verification in column 9, line 47 – column 10, line 4.

24. As per claims 22 and 28, Fruehling et al. discloses coupling a dedicated test-traffic source to the digital data path; providing a first data stream, the first data stream being replicatable; storing a plurality of programmable commands, the programmable commands indicative of at least one of test-traffic type, pattern and behavior; assembling portions of the first data stream into test-traffic wherein at least one of type, pattern and behavior-in-time is selected responsive to the programmable commands; generating test-traffic on the digital data path; monitoring the digital data path for the test-traffic; verifying the monitored test-traffic against a corresponding first data stream; and generating a feedback signal indicative of the test-traffic verification in column 9, line 16 – column 10, line 4. The data generation circuit is the LFSR. The state machine circuitry is the bus control logic. The status and feedback circuit is the parallel signature analyzer.

25. As per claim 23, Fruehling et al. discloses wherein the first data stream is a sequence of pseudo-random numbers each representative of a linear feedback shift register (LFSR) value in column 10, lines 19-33.

26. As per claim 24, Fruehling et al. discloses verifying monitored test-traffic against a corresponding LFSR value, wherein the feedback signal is an interrupt indicative of each test-traffic verification in column 9, line 47 – column 10, line 4.

27. As per claim 25, Fruehling et al. disclose counting a predetermined number of command-execution repetitions; timing each command-execution repetition against an associated programmable period; and generating a feedback signal indicative of a command-execution repetition exceeding the associated programmable period in column 9, line 47 – column 10, line 4.

28. As per claim 27, Fruehling et al. discloses wherein test-traffic type is one of a group consisting of 1, 2, 4, 8, 16, 32, and 64 transfers per burst in column 9, lines 26-34 and column 13, lines 13-28.

Claim Rejections - 35 USC § 103

29. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

30. Claims 18 and 26 rejected under 35 U.S.C. 103(a) as being unpatentable over Fruehling et al. in view of Kim et al. (US Publication Number 20020138678A1). Fruehling et al. fails to explicitly state the digital data path is an AHB protocol bus.

Kim et al. discloses this limitation on page 4, paragraph 0075, "System 400 includes a system bus 410 that can be an advanced microcontroller bus

architecture (AMBA) bus developed, for example, by Advance RISC Machines (ARM) Co. System bus 410 can be made by a advanced high performance bus (AHB)."

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the digital data path be an AHB protocol bus. A person of ordinary skill in the art would have been motivated to have the digital data path be an AHB protocol bus because the AHB bus allows the transfer of data from one device to another. Kim et al. discloses this on page 6, paragraph 0111.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yolanda Wilson whose telephone number is (703) 305-3298. The examiner can normally be reached on M-F (7:30-4:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

DIEU-MINH LE
PRIMARY EXAMINER